Q 61: Trapped lons (joint session Q/A)

Time: Friday 11:00-13:00

Integrated photonics make ion trap setups scalable to large numbers of ions, help to compactify the setup and improve the robustness against vibrations for portable optical clocks and quantum sensors. We are developing ion traps with integrated photonics for quantum metrology. With photonic design structured light can be generated that, combined with improved pointing stability, enables the excitation of forbidden transitions in trapped ions. For the cooling and addressing of Yb⁺ ions wavelengths from UV to NIR are required. The light is coupled in from optical fibers, distributed via waveguides, and coupled out through the surface of the chip via gratings. Our aim is to employ the traps in portable optical clocks that can be used for geodetic measurements.

Q 61.2 Fri 11:30 HS 1199

Apparatus design for scalable cryogenic trapped-ion quantum computing experiments — • TOBIAS POOTZ¹, LUKAS KILZER¹, CE-LESTE TORKZABAN¹, and CHRISTIAN OSPELKAUS^{1,2} — ¹Institut für Quantenoptik, Leibniz Universität Hannover, Welfengarten 1, 30167 Hannover, Germany — ²Physikalisch-Technische Bundesanstalt, Bundesallee 100, 38116 Braunschweig, Germany

Future applications for trapped ion quantum computers require a signicant increase in the number of ion gubits and excellent interconnectivity. In my talk I will describe the design of cryogenic demonstrator machines for this task, implementing surface-electrode ion traps mounted on a universal interchangeable socket. The apparatus design is based on a vibration-isolated cold head to cool a cryogenic vacuum system to temperatures below 10 K. The system features several hundred DC control lines to support transport of qubits through dedicated trap structures including junctions, storage, detection and manipulation registers. Multi-qubit quantum gates will be implemented through the use of chip-integrated microwave lines. The system has been designed to accommodate the integration of new components for scaling as the development of the underlying enabling technologies progresses, such as chip integrated waveguides. Multiple setups were built. One setup is based on 9Be+ qubits and 40Ca+ ions for sympathetic cooling; a second setup will be based on 43Ca+ qubits and 88Sr+ cooling ions.

Q 61.3 Fri 11:45 HS 1199

Fabrication of multisegmented ion traps in a specialized cleanroom — •ALEXANDER MÜLLER¹, JAN MÜLLER¹, BJÖRN LEKITSCH¹, and FERDINAND SCHMIDT-KALER^{1,2} — ¹QUANTUM, Institut für Physik, 55128 Mainz, Germany — ²Helmholtz-Institut Mainz, 55099 Mainz, Germany

Trapped ions are among the leading platforms in quantum computing. We aim to scale up to 50 ions by taking advantage of versatile linear multi-segmented ion traps which combine qubit register reconfigurations [1] and individual addressing of ions in these registers. A fully three-dimensional shaping of electrodes, a homogeneous wellconducting high quality metallic coverage, the precise alignment of trap structures, an excellent optical access, and a fully reliable and repeatable fabrication process are required.

For this we established a special purpose cleanroom. By Selective Laser-induced Etching (SLE) a 3D structure is formed out of fused silica [2]. Metallic sputter deposition results in functional trap chips, which are assembled using a die-bonder, finally fixed on a carrier PCB, and wirebonded for electrical connection of the electrodes. All fabrication steps can be performed in-house and without leaving the Location: HS 1199

clean room in a rapid prototyping fashion (<10 days). We report the testing of devices and the trapping of Ca+ ions.

[1] V. Kaushal et al., AVS Quantum Sci.; 2 (1):014101.

[2] S. Ragg et al., Rev. Sci. Instrum.; 90 (10):103203.

 $\label{eq:generalized_constraints} \begin{array}{c} Q \ 61.4 \ \ {\rm Fri} \ 12:00 \ \ {\rm HS} \ 1199 \\ {\rm Microfabrication \ of \ surface \ ion \ traps \ for \ operation \ with } \\ {\rm Strontium \ Rydberg \ ions \ } & - \ \bullet {\rm Simon \ Schey}^{1,2}, \ \ {\rm Michael} \\ {\rm Pfeifer}^{1,3}, \ {\rm Marion \ Mallweger}^2, \ {\rm Natalia \ Kuk}^2, \ {\rm Ivo \ Straka}^2, \\ {\rm Clemens \ Rössler}^1, \ {\rm Yves \ Colombel}^1, \ {\rm and \ Markus \ Hennrich}^2 \ - \ {}^1 {\rm Infineon \ Technologies \ Austria \ AG, \ Villach, \ Austria \ - \ {}^2 {\rm Stockholm, \ Sweden \ - \ {}^3 {\rm University \ of \ Innsbruck, \ Innsbruck, \ Austria \ } \end{array}$

Recently, using Rydberg-states for gate operation in trapped ions has been shown to greatly reduce two qubit gate times down to 700ns [1]. Those experiments were performed in a macroscopic Paul trap at room temperature. We propose to perform similar experiments but in a cryogenic environment as well as on a of surface ion trap chip that is industrially microfabricated at Infineon Technologies [2,3]. This will prove further scalability of this gate scheme.

As UV-Lasers are needed for the Rydberg gate operation, we discuss material and design choices for making our ion trap resilient against radiation down to a wavelength of around 240nm and show successful microfabrication of an ion trap on a sapphire substrate.

[1] Chi Zhang et al., Nature 580, 345-349 (2020)

- [2] Ph. Holz et al., Adv. Quantum Technol. 3, 2000031 (2020)
- [3] S. Auchter et al., Quantum Sci. Technol. 7, 035015 (2022)

Q 61.5 Fri 12:15 HS 1199 Industrial microfabrication of 2D and 3D ion traps for quantum information processing — •Yves Colombe¹, Silke Auchter¹, Klemens Schüppert¹, Matthias Dietl^{1,2}, Alexander Zesar^{1,3}, Jakob Wahl^{1,2}, Max Glantschnig^{1,4}, Christian Flasch^{1,4}, Simon Schey^{1,5}, Fabian Laurent^{1,6}, Michael Preifer^{1,2}, Fabian Anmasser^{1,2}, Michael Hartmann⁷, Leon Dixius⁷, Mohammad Abu Zahra⁷, Jens Repp⁷, Nina Megier¹, Matthias Brandl⁷, and Clemens Rössler¹ — ¹Infineon Technologies, Villach, Austria — ²University of Insbruck, Innsbruck, Austria — ³University of Graz, Graz, Austria — ⁴PTB, Braunschweig, Germany — ⁵University of Stockholm, Stockholm, Sweden — ⁶Montan University of Leoben, Leoben, Austria — ⁷Infineon Technologies, Oberhaching, Germany

Scaling TIQC to thousands of ions requires microfabricated traps produced in highly reliable facilities. Industrial fabrication provides precise process control as well as in-line measurements tools that ensure high reliability and reproducibility.

Various ion trap designs have been produced at Infineon Technologies cleanroom facilities, including 2D ion trap arrays and 3D traps assembled at wafer level. In this talk I will report on our current work towards large-scale ion traps, including fabrication on dielectric substrates (fused silica, sapphire), through-glass-vias, use of Kelvin probe force microscopy for DC surface potential measurements, integration of fs-laser-written optical waveguides, and development of electronic devices that can operate at 4 K.

Q 61.6 Fri 12:30 HS 1199

Optical integration in ion-trap chips at Infineon — •ALEXANDER ZESAR^{1,2}, JAKOB WAHL^{2,3}, BERNHARD LAMPRECHT⁵, PHILIPP HURDAX⁵, KLEMENS SCHÜPPERT², CLEMENS RÖSSLER², YVES COLOMBE², SILKE AUCHTER², SOFIA CANO CASTRO^{2,6}, MAX GLANTSCHNIG^{2,7}, MARCO SCHMAUSER³, MARCO VALENTINI³, PHILIPP SCHINDLER³, THOMAS MONZ^{3,4}, and JOACHIM KRENN¹ — ¹University of Graz, Graz, Austria — ²Infineon Technologies Austria AG, Villach, Austria — ³University of Innsbruck, Innsbruck, Austria — ⁴Alpine Quantum Technologies GmbH, Innsbruck, Austria — ⁵Joanneum Research Materials, Weiz, Austria — ⁶Polytecnico di Milano, Milan, Italy — ⁷Physikalisch-Technische Bundesanstalt, Braunschweig, Germany

Trapped ions are among the most researched and advanced quantum computing (QC) hardware platforms. Currently used free-space optics for ion addressing will block upscaling due to beam pointing errors and spatial restrictions. Therefore, future QC architectures with trapped

ions require integrated waveguiding and focusing for scalable and stable placement of laser beams in microfabricated ion-trap chips.

This talk gives a concise overview of photonics and optics integration schemes developed at Infineon. We will discuss some of the challenges that come with femtosecond-laser-written waveguides as well as slab waveguides in conjunction with focusing grating couplers, including fiber-to-chip coupling and integration density. The talk concludes with an outlook on scalable ion-trap chips with integrated photonics as a necessary condition for useful trapped-ion quantum computing.

Q 61.7 Fri 12:45 HS 1199

How to Wire a 1000-Qubit Trapped-Ion Quantum Computer — Maciej Malinowski¹, David Allcock^{1,2}, •Clemens Matthiesen¹, and Chris Ballance^{1,3} — ¹Oxford Ionics, Oxford,

 $\rm UK-^2 University$ of Oregon, Eugene, USA — $^3 \rm University$ of Oxford, Oxford, UK

Scaling up quantum computers requires efficient signal delivery to the quantum processor (the "wiring" challenge). It is likely that integration of control electronics into the processor package will be necessary, but this process is heavily constrained by chip microfabrication and chip operation specifications. Here, we present our WISE (Wiring using Integrated Switching Electronics) architecture as an answer to the wiring question, where judicious integration of simple switching electronics into the ion trap chip is combined with parallel trap electrode control [1]. This significantly reduces the number of signal sources needed, such that a fully connected 1000-qubit trapped ion quantum computer might be operated using only ~ 200 signal sources.

[1] M. Malinowski *et al.*, PRX Quantum **4**, 040313 (2023)