T 117: Trigger+DAQ 4

Time: Friday 9:00–10:30 Location: Geb. 30.23: 3/1

T 117.1 Fri 9:00 Geb. 30.23: 3/1

Reconstruction of faint non-standard model particles in IceCube — •Nick Jannis Schmeisser, Timo Stürwald, and Alexander Sandrock — Bergische Universität Wuppertal

The new Faint Particle Trigger (FPT) in IceCube was developed with the intention of reaching a higher sensitivity for faint signals in the IceCube detector. Instead of customary triggers, which are based on local coincidences between two optical modules in the detector, it also uses isolated hits. Therefore, it is especially suited for the search for faint signals in the detector. Examples are fractionally charged particles, which produce less Cherenkov light in comparison to muons because of their smaller charge, or other non-standard model particles.

This presentation shows studies on multiple cleaning and reconstruction approaches in order to develop a reconstruction algorithm for events triggered by the FPT. The discussed algorithms include customary reconstruction techniques used in IceCube, which were adapted to the newly recorded signals, as well as new approaches that use additional information provided by the trigger. Furthermore, reconstruction methods based on machine learning using Graph Neural Networks are applied to the resulting triggered events.

T 117.2 Fri 9:15 Geb. 30.23: 3/1

Development and characterization of a new time reference plane and trigger system for a MIMOSA26 test beam telescope — •Rasmus Partzsch, Christian Bespin, Yannick Dieter, Fabian Hügging, Lars Schall, and Jochen Dingfelder — Physikalisches Institut, University Bonn, Germany

Test beam telescopes facilitate a characterization of different detector parameters and consist of multiple detector planes with high spatial resolution. ANEMONE is a beam telescope, comprising 6 MIMOSA26 planes. Because of the MIMOSA26 readout cycle, multiple hits are included in a single readout frame. To resolve individual tracks within the readout cycle, a reference detector with high precision timestamping capabilities is required. Currently, the ATLAS FE-I4 chip is utilized as such. For the ATLAS inner tracker upgrade, the ITkPix readout chip was developed, featuring a smaller pixel size and the same time resolution as the FE-I4. A replacement with the new ITkPix chip enables a more efficient track reconstruction. Additionally, it can be utilized to provide a region-of-interest trigger in conjunction with the new AIDA TLU. It provides clock and time-stamp synchronization with the DUT and a more complex triggering logic compared to the previously used EUDET TLU. A new Python-based control software for the AIDA TLU has been developed for usage with the ANEMONE beam telescope.

In this talk, the integration of the AIDA TLU into the ANEMONE telescope is demonstrated. In addition, results with the upgraded time reference plane in terms of track reconstruction efficiency are shown.

T 117.3 Fri 9:30 Geb. 30.23: 3/1

ATLAS ITk-Pixel Read-out Chain Stress Test — •Matthias Drescher, Jörn Grosse-Knetter, Arnulf Quadt, and Ali Skaf — II. Physikalisches Institut, Georg-August-Universität Göttingen, Germany

The current ATLAS Inner Detector will be upgraded to an all-silicon Inner Tracker (ITk) for the Phase 2 upgrade of the experiment. The ATLAS ITk readout system uses the FELIX hardware/software system to connect the fibre-optic cables of the on-detector components to the higher-level infrastructure. Each FELIX card has 24 bidirectional high-speed fibre links. In the Pixel subdetector configuration, each uplink fibre is connected to an lpGBT aggregator chip, which in turn bundles 7 Aurora 64b/66b data lanes at 1.28 Gbps. These data are the outputs of the connected front-end chips (RD53A or ITkPix). To ensure stable operation under full load before moving to the final large-scale readout system, a stress test is being prepared populating all 24 FELIX fibres.

Due to limited hardware availability, a stress test setup was prepared using lpGBT and RD53A emulators implemented on several Xilinx FPGA development boards, to be used in place of the respective ASICs. The hit data sent by the RD53A emulators are stored in fast local memory, which can be written from a central controller computer connected to the FPGA boards via Gigabit Ethernet. To implement this Ethernet connection, a processing system is implemented on the FPGA boards, making the design a System-on-Chip (SoC). The project is therefore threefold, consisting of the FPGA design, the SoC processor code and the offline code to control the boards.

T 117.4 Fri 9:45 Geb. 30.23: 3/1

Microservices framework and configuration database for ATLAS ITk — •Jonas Schmeing, Gerhard Brandt, Marvin Geyik, Maren Stratmann, and Wolfgang Wagner — Bergische Universität Wuppertal

For the LHC Phase-2 upgrade, a new inner tracker (ITk) will be installed in the ATLAS experiment. It will allow for even higher data rates and will be thoroughly tested in the ATLAS ITk system tests. To operate these tests and later the final detector, a GUI and configuration system is needed. For this a flexible and scalable framework based on distributed microservices has been introduced. Different microservices are responsible for configuration or operation of all the parts in the readout chain.

The configuration database microservice provides the configuration files needed to configure the hardware components of the readout chain and perform scans. It saves all the connectivity information and configuration files needed to operate the system in so called runkeys, who are saved in a flexible, tree-based data structure. This flexible structure the runkeys allows the storage of specialized runkeys made up of different objects for the ITk subdetectors.

To efficiently serve these files to the subdetectors, a distributed system of ConfigDB caches is introduced. The master instance of the ConfigDB provides these caches with subsets of the runkeys depending on the elements of the readout chain that the specific cache serves.

T 117.5 Fri 10:00 Geb. 30.23: 3/1

OSIRIS DAQ: Design and Commissioning — •Arshak Jafar, Michael Wurm, Oliver Pilarczyk, Tim Charisse, Marcel Buchner, and George Parker — JGU Mainz, Institute of Physics and EC PRISMA+

The Jiangmen Underground Neutrino Observatory (JUNO), under construction in southern China, will determine the neutrino mass hierarchy (MH) by observing neutrinos from nuclear reactors at a distance of 53 km. To reach the desired sensitivity ($> 3\sigma$) for MH, the radiopurity of the different detector components plays a crucial role. To ensure the purity of the 20 kt liquid scintillator (LS) target of JUNO, the Online Scintillator Internal Radioactivity Investigation System (OSIRIS) is being constructed. The 20-ton pre-detector will monitor the radiopurity of the LS during its production and the filling phase of the central detector of JUNO.

This talk will focus on the design principles and working of the data acquisition system (DAQ) of the OSIRIS pre-detector as well as the details on commissioning that has been done over the past year leading to the first data.

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T 117.6 Fri 10:15 Geb. 30.23: 3/1

The build system for the *Mu3e* DAQ firmware — •Alexandr Kozlinskiy — Institut für Kernphysik, JGU Mainz

The *Mu3e* experiment is designed to search for the lepton flavor violating decay $\mu^+ \to e^+e^-e^+$ with the aim of reaching a branching ratio sensitivity of 10^{-16}. The experiment is located at the Paul Scherrer Institute (Switzerland). The existing beam line will provide 10^8 muons per second and at first will allow to reach a sensitivity of a few 10^{-15}.

The readout system of *Mu3e* utilizes Intel FPGA chips for which the firmware and IP components are compiled with the Quartus software package. To streamline the development and testing of the *Mu3e* DAQ firmware, custom scripts and tools were developed to allow for building and testing of the firmware directly from the command line and on the continuous integration server where firmware for all subsystems is built on each commit. This allowes for faster iteration on firmware designs and better tracking of regressions during development.

The talk will present the scripts and tools, and the overall design of the build system for the *Mu3e* DAQ firmware.