T 12: Detectors 1 (electronics)

Time: Monday 16:00–17:45 Location: Geb. 30.23: 2/1

T 12.1 Mon 16:00 Geb. 30.23: 2/1

SIPM based cosmic muon detector wih FPGA implemented digitization — •Erik Ehlert, Dmitry Eliseev, Carsten Presser, Markus Merschmeyer, and Thomas Hebbeker — III. Physikalisches Institut A, RWTH Aachen University

A cosmic muon hodoscope which is to be used as a reference detector was designed and is undergoing the first performance tests. This hodoscope consists of an array of scintillator strips which are each coupled to a pair of Silicon-Photomultipliers (SiPMs). The signal digitization is performed directly with a Field-Programmable Gate Array (FPGA). This is achieved by using a Multi-Voltage Thresholding (MVT) approach utilizing solely FPGA's internal comparators, effectively implementing a flash ADC. With this setup a sampling rate of 800 Megasamples per second is reached.

The talk provides an overview of the detector setup, including technical design and electronic readout chain. Performance characteristics of the detector are presented as well.

T 12.2 Mon 16:15 Geb. 30.23: 2/1

Verification of the new CMS DT on-chamber electronics — •Dmitry Eliseev, Matej Repik, Carsten Presser, Markus Merschmeyer, and Thomas Hebbeker — III. Physikalisches Institut A, RWTH Aachen University

The Compact Muon Solenoid (CMS) is undergoing the Phase 2 Upgrade, including improvements to the muon-detecting drift tube chambers (DT). The upgrade involves replacing the legacy on-chamber DT electronics with the recently developed On-Board Drift Tube (OBDT) electronics. While moving towards the production and assembly phase, comprehensive quality assurance for the new OBDT electronics gains priority. The CMS DT collaboration developed instruments for testing and verification of the new electronics. These instruments will be deployed at different sites throughout the CMS DT collaboration. This talk gives an overview of the verification setups and methods and presents some initial verification results.

T 12.3 Mon 16:30 Geb. 30.23: 2/1

Irradiation test campaign on the CMOS LDO components for the ATLAS sMDT on-detector electronics for the HL-LHC Phase-II Upgrade — Sergey Abovyan, Nayana Bangaru, •Francesco Fallavollita, Markus Fras, Oliver Kortner, Sandra Kortner, Hubert Kroha, Robert Richter, and Elena Voevodina — Max Planck Institut für Physik - Werner Heisenberg Institute, München, Germany

The Muon System of the ATLAS experiment at CERN LHC will be upgraded for the high-luminosity phase of LHC to cope with higher rates and higher radiation levels. Most of the Muon-System on-detector electronics will be replaced. Commercial low-dropout (LDO) voltage regulators have been considered as a robust, low-noise and economic solution to power distribution in the ATLAS sMDT front-end electronics for the HL-LHC Phase-II Upgrade. The LDO components should be selected based on their capability to comply to radiation requirements. For this reason, radiation hardness studies have been extensively performed on different production batches of CMOS LDOs, by constantly monitoring online the relevant parameters during the TID and SEE irradiation test. Irradiations were performed in the Cobalt-60 facility at CERN (Geneva), to test resistance to the TID effects, and at the Proton Irradiation Facility 230 MeV proton beam at PSI (Zurich), to test SEE effects. Additionally, a post radiation accelerated annealing test has been performed on the irradiated samples in order to study any potential long term effects. The experimental setup and the results are presented and discussed in this communication.

T 12.4 Mon 16:45 Geb. 30.23: 2/1

Towards a High-Performance Readout System for the CMS High Granularity Calorimeter — •Fabian Hummer, Luis Ardila, and Frank Simon — Karlsruhe Institute of Technology

For the upcoming high-luminosity LHC, the endcap calorimeters of the CMS experiment will be replaced by the high granularity calorimeter (HGCAL), one of the most ambitious detector projects undertaken. Due to the extremely high number of readout and trigger channels, in combination with a high event rate and pile-up, HGCAL requires a high-performance, FPGA-based readout system. Collaborating closely with CERN, DESY and Imperial College London, the CMS group at the Institute for Data Processing and Electronics (IPE) at KIT contributes both to development of firmware and software for the readout and control of HGCAL, as well as to the design of the new Serenity-S1 hardware. In this contribution I will discuss how we address the challenges in data readout that we are facing for HGCAL, and highlight the contributions from IPE at KIT.

T 12.5 Mon 17:00 Geb. 30.23: 2/1

Code-driven analog design for detector readout ASICs — •Kennedy Caisley, Marco Vogt, Hans Krüger, and Jochen Dingfelder — University of Bonn, Bonn, Germany

Readout integrated circuits for pixelated radiation detectors have experienced a renaissance in the past two decades, with over 50 full-reticle chip designs reported in the HEP and photon science communities alone. The adoption of smaller process nodes (from 350 nm down to 28 nm) has generally improved performance, density, and power efficiency; but at the cost of increased design effort.

This talk describes workflows using programming languages like Python, C++, and Rust to design analog readout circuits. Procedural-style code is well-suited for automating 'bottom-up' tasks like schematic device sizing, layout generation, and analysis of SPICE simulation, while 'top-down' optimization routines suitably formalize constraints like silicon area and power consumption.

T 12.6 Mon 17:15 Geb. 30.23: 2/1

Investigation of the Belle II Pixel Detector Power Supply Network — Patrick Ahlburg, Florian Bernlochner, Jochen Dingfelder, Hans Krüger, •Botho Paschen, and Paula Scholz — University of Bonn

The Belle II PiXel Detector (PXD) is based on modules with DEpleted P-channel Field Effect Transistor (DEPFET) sensors. Each module is powered by 23 dedicated power supply channels. Since the Power Supplies (PS) are located outside the Belle II detector, 15 m long cables and several decoupling capacitor stages are necessary in the powering path.

To better protect modules in case of beam loss events an active shutdown procedure is proposed. In addition to PS regulators shutting down, nets on the PS side are actively shorted by switches to reduce voltage settling times.

Because of the complicated powering path structure a dedicated characterization and simulation of all system components is necessary for a successful implementation of the active shutdown. The status of the investigations using different measurement and simulation tools (a.o. time domain reflectometry, network analyzer, LTspice, HyperLynx) are presented in this talk.

T 12.7 Mon 17:30 Geb. 30.23: 2/1

New amplifier-shaper discriminator chip in 65 nm CMOS technology for small-diameter muon drift-tube chambers at future hadron colliders — •Nayana Bangaru, Sergey Abovyan, Francesco Fallavollita, Oliver Kortner, Sandra Kortner, Hubert Kroha, Giorgia Proto, Robert Richter, Elena Voevodina, and Yazhou Zhao — Max-Planck-Institut für Physik (Werner-Heisenberg-Institut), Garching, Germany

Small-diameter muon drift tubes (sMDT) are used for large area muon detection in the ATLAS experiment at HL-LHC and have been proposed for muon tracking and triggering at future hadron collider experiments. sMDTs have been shown to operate with high spatial resolution and efficiency up to a gamma background count rate of 30 kHz/cm^2. The background count rates in the muon systems at Future Circular Colliders like the FCC-hh are expected to be 10 kHz/cm^2 for $|\eta| \leq 2.0$ and up to 25 kHz/cm^2 at $|\eta| \approx 2.5$.

With the new ATLAS ASD chip for operation at HL-LHC, a single tube resolution of 150 micrometers is reached at a counting rate of about 7 kHz/cm^2. In order to achieve the required muon angular resolution of 70 μrad at the FCC-hh, the spatial resolution needs to be improved by suppressing signal pile-up. A new ASD chip in 65nm CMOS technology has been developed with faster baseline recovery which improves the spatial resolution and increases the efficiency at high rates by reducing the dead time by 50%. Performance of the new chip was tested on a sMDT chamber at the CERN GIF++ gamma irradiation facility in comparison with the ATLAS chip.