T 34: Data, AI, Computing, Electronics IV (DAQ, Detector Electronics)

Time: Tuesday 16:15–18:15 Location: VG 2.102

T 34.1 Tue 16:15 VG 2.102

FPGA-Based Solution Beyond High-Speed ADCs for Particle Detectors — •Dmitry Eliseev, Erik Ehlert, Carsten Presser, Markus Merschmeyer, Alexander Schmidt, and Thomas Hebbeker — III. Physikalisches Institut A, RWTH Aachen University

Modern particle detector electronics often handle a big number of channels. Field Programmable Gate Arrays (FPGAs) often serve as the core engine of multi-channel acquisition systems. However, the standard approach for acquiring energy or amplitude information for specific events often relies on high-speed multi-channel ADCs. Using such ADCs can increase complexity and raise the cost of signal acquisition electronics. The Multi-Voltage-Thresholding (MVT) method utilizes the internal digital comparators of FPGAs, partially replacing the functionality of ADCs with FPGA-internal resources. This approach enables a fast multi-channel acquisition, which is solely FPGA-based. By eliminating the need for external high-speed multi-channel ADCs, the resulting schematics are simplified, and the cost of the detector electronics is reduced.

This talk explains the MVT methodology and demonstrates its practical application using a 16x16 pixel muon detector with 64 Silicon Photo-Multipliers (SiPMs). The developed system is based on commercially available modules with System-on-Chip (Zynq MPSoC). With compact additional circuitry and developed soft- and firmware, the system features up to 16 high-speed ADC channels, each sampling at 1 GSPS and delivering the sampled data directly to module's RAM.

T 34.2 Tue 16:30 VG 2.102

The ATLAS Tile Calorimeter Trigger and Data Acquisition Interface — •Thomas Junkermann and Tigran Mkrtchyan — Kirchhoff-Institut für Physik Heidelberg

The Phase-II Upgrade of the ATLAS Tile Calorimeter (TileCal) is a replacement of the entire on- and off-detector electronics to cope with the higher amount of simultaneous proton-proton collisions of future LHC runs. New back-end electronics are designed to provide high-bandwidth data to the new Phase-II Trigger and Data Acquisition (TDAQ) system. The Tile Calorimeter Trigger and Data Acquisition Interface (TDAQi) is an ATCA rear transition module and as part of the new TileCal PreProcessor serves as the connection between the off-detector calorimeter electronics and the TDAQ system of ATLAS. After the calorimeter cell signals are received and energies reconstructed by the Compact Processor Modules, the TDAQi prepares the data for further use. Cell energies are converted to transverse energy, cells are sorted or added to larger sums for the trigger and various threshold comparisons for muon candidate identification are provided. Additionally, the TDAQi forwards these intermediate results to the DAQ system for monitoring. The TDAQi as part of the ATLAS Phase-II upgrade will be presented. Together with latest hardware validation and integration tests, the general TDAQi status is featured.

T 34.3 Tue 16:45 VG 2.102

Towards Data Transfer and Monitoring Interfaces for the future Signal Processor of the ATLAS Liquid Argon Calorimeters — •Markus Helbig, Rainer Hentges, Arno Straessner, Johann Christoph Voigt, and Philipp Welle — Institut für Kern- und Teilchenphysik, TU Dresden

During the Phase-II Upgrade of the ATLAS Liquid Argon Calorimeter System, the new LAr Signal Processor (LASP) system will be installed. With the HL-LHC starting operation in 2030, this off-detector processing system will enable the use of novel, more powerful algorithms for energy reconstruction implemented on Intel Agilex 7 FPGAs.

Beside the main readout path, the LASP will provide fine granular and pre-summed energies and energy threshold values to two new ATLAS trigger systems – the Global Event Processor (GEP) and the Forward Feature Extractor (fFEX). For both interfaces, the preferred protocol candidate is the Interlaken-based *core1990*, operating at a speed of 25.78125 Gbps. Its functionality and properties are currently being verified on the Agilex 7 FPGA.

Additionally, the LASP firmware will also contain several registers for control and monitoring purposes. The implementation is based on the *IPbus* protocol embedded in a custom framework. The physical connections are realized using a Gigabit Ethernet interface.

The presentation will summarize the challenges, recent progress and results of the LASP interface projects.

T 34.4 Tue 17:00 VG 2.102

Firmware development for temperature monitoring of electro-optical transceivers for the ATLAS Liquid Argon Signal Processor system — •Peter Maximilian Fischer, Markus Helbig, Rainer Hentges, and Arno Straessner — Institut für Kern- und Teilchenphysik, TU Dresden

As part of the Phase-II upgrade of the ATLAS detector, its Liquid Argon (LAr) calorimeters will be equipped with a new Signal Processor (LASP) system following the high luminosity upgrades to the LHC. The data transfer coming from the Front End Board (FEB2) to the LASP and going from the LASP to the ATLAS trigger system will be handled by electro-optical transceivers of type SAMTEC Firefly, which will have to be monitored with regards to their temperature by an FPGA. For this purpose, an I^2C master has been interfaced in VHDL. A simulation in QuestaSim as well as hardware testing with a Stratix-10 FPGA on a Firefly test card and a LASP testboard were performed in order to verify the desired behaviour, with a test on an Agilex-7 based LASP testboard pending. The results and conclusions from these tests will be presented, as well as an outlook towards the implementation of a Serial Peripheral Interface (SPI) for the communication between the Agilex-7 and MAX-10 FPGAs.

T 34.5 Tue 17:15 VG 2.102

DAQ software for QC-tests of ATLAS ITk-Pixel loaded local supports — Jörn Grosse-Knetter, •Paolo Malatesta, Arnulf Quadt, and Ali Skaf — II. Physikalisches Institut, Georg-August-Universität Göttingen, Friedrich-Hund-Platz 1, 37077 Göttingen

The increase of luminosity at the ATLAS Large Hadron Collider (LHC), previewed in the phase 2 upgrade, will require an update of the ATLAS inner detector. A new all-silicon Inner Tracker (ITk) will be deployed resulting in an increased data rate. The 5 billion pixels comprise over 9,000 Quad Modules (QMs), which are managed by the DAQ system via FELIX hardware/software. In the ITk outer barrel, QMs send 1.28 Gb/s electrical signals to the Optoboard for conversion to optical signals, which are then transmitted off-detector to FELIX PCs and the DAQ software. The reverse path is used for QM Front-End (FE) configuration and control. To validate the DAQ system's readiness for the upgrade, a lab setup reproducing the FELIX/optoboard readout chain was tested with preproduction QMs using serial powering. Simultaneous readout enabled analysis of system behaviour under load, identifying key parameters for signal quality and reliability. DAQ performance, including configuration time, was measured as a function of enabled FEs, providing insights crucial for scaling the DAQ chain to large systems like the local supports loaded with few 10 modules and the full ITk-pixel DAQ.

T 34.6 Tue 17:30 VG 2.102

ATLAS ITk-Pixel read-out stress tests — •Matthias Drescher, Jörn Grosse-Knetter, Arnulf Quadt, and Ali Skaf — II. Physikalisches Institut, Georg-August-Universität Göttingen

The current ATLAS Inner Detector will be upgraded to an all-silicon Inner Tracker (ITk) for the Phase 2 upgrade of the experiment. The ATLAS ITk readout system is based on the FELIX hardware/software used to interface the on-detector components from the higher-level DAQ infrastructure. One FELIX card has 24 optical fibre links, which are fanned out to multiple Pixel modules by the lpGBT aggregator chip. To ensure stable operation under full load before moving to the final large-scale readout system, a stress test is being prepared populating all 24 FELIX fibres.

The data generation for the stress test takes place on several AMD FPGA boards, each containing multiple instances of lpGBT and front-end chip emulators. For this project, multiple front-end emulator flavours are developed to generate data streams according to the ITkPix production chip or the RD53A prototype chip data format. The front-end emulators use a hybrid design, where the test data is partially encoded off-FPGA and then stored in the FPGA's memory, to be fully encoded by the FPGA logic. As such, the project consists of both the FPGA design and the external software written in Python, which prepares the test data and automates the tests. Tests have been

performed with both types of emulator flavours.

T 34.7 Tue 17:45 VG 2.102

Integration of SiPM-on-Tile Detectors with the Serenity Phase-2 DAQ Hardware for the CMS High Granularity Calorimeter — •Fabian Hummer[1], Luis Ardila-Perez[1], Matthias Balzer[1], Marvin Fuchs[1], Olivier Jacquemoth[1], Matthias Komm[2], Hendrik Krause[1], Katja Krüger[2], Jia-Hao Li[2], Torben Mehner[1], Mathias Reinecke[2], Frank Simon[1], Felix Sefkow[2], and Raghunandan Shukla[3] — [1]Institute for Data Processing and Electronics, Karlsruhe Institute of Technology, Hermann-von-Helmholtz-Platz 1, 76344 Eggenstein-Leopoldshafen, Germany — [2]Deutsches Elektronen-Synchrotron DESY, Notkestraße 85, 22607 Hamburg, Germany — [3]Department of Physics, Imperial College London, Exhibition Road, London, SW7 2BW, United Kingdom

For the upcoming high-luminosity LHC, the endcap calorimeters of the CMS experiment will be replaced by the high-granularity calorimeter (HGCAL), a sampling calorimeter using both silicon and scintillator as active materials in different regions depending on the radiation dose. This contribution describes the integration details of the scintillator-based front-end into the DAQ readout chain of HGCAL utilizing a Serenity FPGA card. Initial results from a beam test at CERN showcase stable operation of the SiPM-on-tile front-end in a 3 T magnetic field, synchronization of multiple tile modules, as well as a good understanding of the relation between trigger and DAQ data with properly calibrated modules.

T 34.8 Tue 18:00 VG 2.102

Development of a standalone drift-tube-based muon trigger for the ATLAS and CRESST experiments — D Cieri, •S Eder, O Kortner, S Kortner, A Langenkämper, M Mancuso, and F Petricca — Max Planck Institut für Physik, Garching, Germany

To operate the ATLAS experiment in the high-rate environment of the High-Luminosity Large Hadron Collider (HL-LHC), significantly improved selectivity of the first-level muon trigger is required. To achieve this, novel FPGA-based Monitored Drift Tube (MDT) trigger processor boards have been developed. These boards incorporate muon tracking information from precision MDT chambers into the first-level trigger processing chain for the first time. The new MDT chamber read-out and trigger processors must be commissioned using cosmic ray muons, necessitating the development of a dedicated muon track-finding algorithm that utilizes only information from drift-tube detectors.

This algorithm could potentially also be used to build a muon veto trigger for the CRESST experiment at Gran Sasso. The proposed experimental setup involves placing several spare MDT chambers from the ATLAS experiment around the cryogenic crystals of the CRESST detector. Events with cosmic muon tracks can then be vetoed if the signal in the crystals matches the signal from the MDT chambers, significantly reducing the experiment's output bandwidth.

In this talk, a dedicated standalone drift-tube-based muon trigger algorithm will be presented, along with its implementation in the FPGA firmware.