T 5: Silicon Detectors I (ATLAS + CMS)

Time: Monday 16:45–18:15 Location: VG 0.111

T 5.1 Mon 16:45 VG 0.111

The operational experience and performance of the ATLAS SCT during LHC Run-3 operations — •Alessandro Guida — Humboldt University, Berlin, Germany

The ATLAS SemiConductor Tracker (SCT) restarted operations in LHC Run-3. The SCT successfully operated in LHC Run-2 (2015-2018) which came with high instantaneous luminosity and pileup conditions that were far in excess of what the SCT was originally designed to meet. Similar conditions are now faced during the on-going Run-3 and first significant effects of radiation damage in the SCT are observed.

This talk will summarise the operational experience, challenges and performance of the SCT during the first years of Run-3 operations. The observation and prospect of radiation damage on SCT silicon strip sensors will also be presented.

T 5.2 Mon 17:00 VG 0.111

Thermal cycling in Aachen and grading procedures for 2S modules for the CMS Phase-2 Tracker Upgrade — •Max Beckers[2], Lutz Feld[1], Nina Höflich[2], Katja Klein[1], Martin Lipinski[1], Alexander Pauls[1], Oliver Pooth[2], Nicolas Röwert[1], Vanessa Oppenländer[1], and Lennart Wilde[2] — [1]I. Physikalisches Institut B, RWTH Aachen University — [2]III. Physikalisches Institut B, RWTH Aachen University

For the CMS Phase-2 Outer Tracker upgrade, new silicon strip detector modules consisting of two silicon strip sensors, so-called 2S modules, are developed and produced. This process is distributed along multiple assembly centers worldwide.

RWTH Aachen University will build around 1000 2S modules. The assembled modules are then shipped to DESY, where they are thermally cycled in the "Burn-in" setup. In addition, a multi module cold box is available in Aachen to perform thermal cycles for up to 4 modules.

The POTATO software is the centrally developped software to validate the test results and apply the grading procedures. The gradings are based on different electrical and readout parameters of the module and then stored in the central database.

This talk presents the cold box setup at Aachen together with cyclings performed on preproduction 2S modules. In addition to the cycling results, the grading procedures are explained, and the POTATO software is presented.

T 5.3 Mon 17:15 VG 0.111

Thermal qualification of the silicon detector modules for the Phase-2 upgrade of the CMS Outer Tracker — •Niyathikrishna Meenamthuruthil Radhakrishnan, Alexander Dierlamm, Ulrich Husemann, Markus Klute, Stefan Maier, Lea Stockmaier, Tobias Barvich, and Bernd Berger — Karlsruhe Institute of Technology, Karlsruhe, Germnay

The LHC is about to enter its high-luminosity era in 2029. In order to prepare the particle detectors to deal with the high particle rate and radiation damage, the detector components must be upgraded. One upgrade project is the replacement of the tracking system of the CMS detector. The new Outer Tracker will consist of two types of silicon sensor modules: 5592 PS modules which are made of one pixel sensor and one strip sensor and 7608 2S modules with two strip sensors.

Production and testing of these modules are carried out at 10 sites and one of the centers producing the 2S modules is KIT. In the tracker, these modules will be operated with a coolant temperature of around -35. It must be verified that the modules can function flawlessly at this temperature prior to installation in the detector. In order to do that, modules are placed inside a thermally insulated box with active cooling, called burn-in station, to perform temperature cycles and expose the modules to thermal stress for up to 48 hours. The electrical functionality of the modules is monitored during this period.

The talk will give a summary of the current status of the burn-in station at KIT and present the thermal qualification of the station as well as results with the first production modules.

T 5.4 Mon 17:30 VG 0.111

ITk Pixel DCS: Pixel System Monitoring Readout — •Anne Gaa and Stan Lai — Friedrich-Hund Platz 1, 37077 Goettingen

The ATLAS experiment is developing the new Inner Tracker (ITk) in preparation for the High-Luminosity LHC Upgrade. The ITk pixel Outer Barrel demonstrator, as a system prototype, recently passed its final design review phase in preparation of the construction of the finished detector. The Detector Control System (DCS) is responsible for monitoring and controlling the detector and its sub-systems.

Part of the DCS is the readout chain of the Monitoring of Pixel System (MOPS), which provides an independent monitoring of the temperature and voltage of the front-end pixel modules. The MOPS-Hub is the bidirectional interface between the local DCS station and the MOPS chips. The MOPS chips are connected via CAN buses to an FPGA, which sends the monitored data over an OPC UA server to the local DCS control station. Testing sites for the Outer Barrel local supports, as well as the OB demonstrator will use the next iteration of the MOPS readout in the near future, featuring a new FPGA and a new OPC UA server. The OPC UA server will gain the functionality to read and write to the shared register on the FPGA via its device classes. As a first step, this server will be developed in the environment of a register simulation. This talk presents new developments of the MOPS readout.

T 5.5 Mon 17:45 VG 0.111

Testing of ATLAS ITk pixel detector modules — Markus Cristinziani[1], Qader Dorosti[1], •Luke Hammer[1], Stefan Heidbrink[2], Lasse Jäderberg[1], Nils Krengel[1], Nico Malinowski[1], Denise Müller[1], Jason Müller[1], Noah Siegemund[1], Waldemar Stroh[2], Wolfgang Walkowiak[1], Jens Winter[2], Michael Ziolkowski[2], and Alessia Zuev[1] — [1]Experimentelle Teilchenphysik, Center for Particle Physics Siegen, Universität Siegen — [2]Elektronikentwicklungslabor Physik, Universität Siegen

The upcoming High-Luminosity LHC upgrade will significantly increase the LHC's instantaneous luminosity by a factor of 5 starting in 2030. The ATLAS detector upgrade introduces a comprehensive, all-silicon inner tracking system (ITk), comprising sophisticated silicon strip and pixel modules that will completely replace the existing Inner Detector. At the University of Siegen, modules of the Outer Barrel Pixel detector will be assembled and tested, requiring complex setups and intensive quality control procedures to ensure the precision, functionality and reliability of each detector module. In this talk these test setups will be presented. They comprise a comprehensive electrical testing system with integrated interlock mechanisms to protect module integrity during characterization, and a sophisticated thermocycling setup designed to assess module performance after extreme temperature variations.

T 5.6 Mon 18:00 VG 0.111

Quality Control Tests of ITK Pixel Modules — •Ruben Förster, Jörn Grosse-Knetter, and Arnulf Quadt — II. Physikalisches Institut, Georg-August-Universität Göttingen

The High Luminosity upgrade of the Large Hadron Collider (HL-LHC) presents significant challenges for the subcomponents of the ATLAS experiment. Consequently, it necessitates the construction of an all-silicon Inner Tracker (ITk) able to deal with increased particle fluxes and radiation levels.

ITk will feature both hybrid pixel and strip detectors, with the pixels forming the inner part. The ITk pixel detector will consist of about 10,000 separate modules, with approximately 600 of them expected to be processed at the University of Göttingen.

Performing Quality Control (QC) tests is vital to ensure the performance of the modules at the time of installation and during the promised 10 years of operation. The QC tests evaluate the overall functionality and electrical properties of the modules, as well as the performance of individual pixels. QC tests are conducted at different stages of the production process to ensure that the modules are within the specifications and that no damage has occurred during the previous assembly steps. As part of the preproduction phase, work has been undertaken to ensure the feasibility of performing QC tests while also automating and optimizing the processes to ensure that modules can be produced in a timely manner.